



Lynne D. Anderson
Phone 202/775-5763
Fax 202/638-4810
anderson.lynn@arentfox.com
www.arentfox.com

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Dear Examiner Colon:

Per our telephone conference on April 23, 2003, attached is a copy of the postcard and copies of the translations of the priority documents, which you stated were not received. Please contact us if you have any further questions.

Very truly yours,

Lynne D. Anderson

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Arent Fox Kintner Plotkin & Kahn, PLLC
1050 Connecticut Avenue, NW, Washington, D.C. 20036-5339

I, Tetsuo YAMATO

residing at 7-4 Kamisaginomiya 2-chome, Nakano-ku, Tokyo, Japan

Being competent in the Japanese and English language, certify that to the best of my knowledge and belief the attached English translation is a true and faithful translation made by me of Japanese Patent Application No. 2000-229082 filed on July 28, 2000.

Dated: February 13, 2003

A handwritten signature in cursive script, reading "Tetsuo Yamato", written in black ink.

Tetsuo YAMATO

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 [Inventor]
 [Inventor]
 [Address] c/o. Koufu-Jigyosho, Shizuoka Pioneer Corporation,
 2680, Nishihanawa, Tatomicho, Nakakoma-gun, Yamanashi-ken Japan
 [Name] Kimio AMEMIYA
 [Inventor]
 [Address] c/o. Koufu-Jigyosho, Shizuoka Pioneer Corporation,
 2680, Nishihanawa, Tatomicho, Nakakoma-gun, Yamanashi-ken Japan
 [Name] Nobuhiko SAEGUSA
 [Patent Applicant]
 [Identified Number] 000005016
 [Name] Pioneer Corporation
 [Patent Applicant]
 [Identified Number] 398050283
 [Name] Shizuoka Pioneer Corporation
 [Agent]
 [Identified Number] 100063565
 [Patent Attorney]
 [Name] Nobukiyo KOBASHI
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[Title of the Invention] PLASMA DISPLAY PANEL

[Scope of the claimed Patent]

[Claim 1] A plasma display panel including a front substrate and a back substrate on opposite sides of a discharge space, a plurality of row electrode pairs extending in a row direction and arranged in a column direction on the front substrate to form display lines, a protective dielectric layer provided on a face of the front substrate facing the discharge space, a plurality of column electrodes extending in the column direction and arranged in the row direction on the back substrate to form a unit light emitting area in the discharge space at each intersection with the row electrode pair, and a phosphor layer on a face of the back substrate facing the discharge space, said plasma display panel characterized in that:

a secondary electron emissive layer, which is formed of a material having a coefficient of secondary electron emission higher than that of dielectrics forming said protective dielectric layer, is placed at a site facing each unit light emitting area between the front substrate and the back substrate.

[Claim 2] The plasma display panel according to claim 1, wherein said secondary electron emissive layer extends in the row direction at each site opposing the row electrode pairs, and faces toward the discharge space of the unit light emitting areas adjacent to each other in the column direction.

[Claim 3] The plasma display panel according to claim 1, wherein said secondary electron emissive layer extends in the column direction at each site between the unit light emitting areas adjacent to each other in the row direction, and faces toward the discharge space of the unit light emitting areas adjacent to each other in the row direction.

【Claim 4】 The plasma display panel according to claim 1, wherein a partition wall, which includes a transverse wall section extending in the row direction and a vertical wall section extending in the column direction and is disposed between the front substrate and the back substrate, partitions the discharge space into the unit light emitting areas, and said secondary electron emissive layer is provided between the front substrate and the transverse wall section of the partition wall.

【Claim 5】 The plasma display panel according to claim 1, wherein a partition wall, which includes a transverse wall section extending in the row direction and a vertical wall section extending in the column direction and is disposed between the front substrate and the back substrate, partitions the discharge space into the unit light emitting areas, and said secondary electron emissive layer is provided between the front substrate and the vertical wall section of the partition wall.

【Claim 6】 The plasma display panel according to claim 1, wherein a stripe-patterned partition wall is disposed between the front substrate and the back substrate and extends in the column direction for partitioning the discharge space into the unit light emitting areas aligned in the column direction, and said secondary electron emission layer extends in the row direction at a site opposing main bodies of the row electrodes.

【Claim 7】 The plasma display panel according to claim 1, wherein said phosphor layer contains the material, having a coefficient of secondary electron emission higher than that of the dielectrics forming said protective dielectric layer, to be formed in combination with said secondary electron emissive layer.

【Claim 8】 The plasma display panel according to claim 1, wherein an ultraviolet region light emissive layer, which is formed of an ultraviolet region light emitting phosphor

having persistence characteristics allowing continuous radiation of ultraviolet light as a result of excitation by ultraviolet rays having a predetermined wavelength, or a visible region light emissive layer, which is formed of a visible region light emitting phosphor having persistence characteristics allowing continuous radiation of visible light as a result of excitation by ultraviolet rays having a predetermined wavelength, are placed at a site facing each unit light emitting area between the front substrate and the back substrate.

[Claim 9] The plasma display panel according to claim 8, wherein said phosphor layer contains the ultraviolet region light emitting phosphor or the visible region light emitting phosphor to be formed in combination with said ultraviolet region light emissive layer or the visible region light emitting phosphor layer.

[Claim 10] The plasma display panel according to claim 8, wherein the ultraviolet region light emitting phosphor forming said ultraviolet region light emissive layer or the visible region light emitting phosphor forming said visible region light emissive layer is a light emissive material having persistence characteristics allowing radiation for 0.1 msec or more.

[Claim 11] The plasma display panel according to claim 1, wherein said secondary electron emissive layer contains an ultraviolet region light emitting phosphor having persistence characteristics allowing continuous radiation of ultraviolet light as a result of excitation by ultraviolet rays having a predetermined wavelength, or a visible region light emitting phosphor having persistence characteristics allowing continuous radiation of visible light.

[Claim 12] The plasma display panel according to claim 1, wherein said phosphor layer is formed of a light emissive

material having persistence characteristics allowing radiation for 0.1 msec or more.

[Claim 13] The plasma display panel according to claim 8, wherein a light absorption layer is provided at each position opposing a non-lighting area between the unit light emitting areas adjacent to each other in the row direction or the column direction of the front substrate, and opposite the back substrate in relation to said ultraviolet region light emissive layer or visible region light emissive layer.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The invention relates to a plasma display panel of a matrix display scheme.

[0002]

[Problems to be solved by the Invention]

Recent years, a plasma display panel of a matrix display scheme (hereinafter referred to as "PDP") has been received attention as an oversized and slim display for color screen.

[0003]

An AC type PDP is known as such display panels of the matrix display scheme.

[0004]

The AC type PDP includes a plurality of row electrode pairs arranged on the inner face of a front substrate so that each forms a display line, and a plurality of column electrodes arranged on the inner face of a back substrate, opposing the front substrate with a discharge space between, in a direction perpendicular to the row electrode pairs. At each intersection of the row electrode pairs and the column electrodes, discharge cells form a matrix in cooperation with each other.

[0005]

The row electrode pairs and the column electrodes are

overlaid with dielectric layers at the respective surfaces facing the discharge space. Phosphor layers are provided on the column electrodes arranged on the inner face of the back substrate.

[0006]

One of conventionally known methods of displaying a halftone on such a PDP is a so-call sub-field method in which a display period of one field is divided into N sub-fields in which light is emitted at intervals corresponding to the weight of each bit position of the N-bit display data.

[0007]

In the sub-field method, each sub-field consists of a concurrent reset period R_c , an addressing period W_c and a sustain discharge period I_c as illustrated in Fig. 12.

[0008]

In the concurrent reset period R_c , reset pulses RP_x , RP_y are concurrently applied between the row electrodes X_{1-n} and Y_{1-n} paired with each other to produce discharge in all the discharge cells in unison, thereby temporarily forming a predetermined amount of wall charge in each discharge cell.

[0009]

In the addressing period W_c , scan pulses SP are sequentially applied to the row electrodes Y_{1-n} each which is one of the row electrode pair, and display data pulses DP_{1-n} corresponding to the display data in each display line are applied to the column electrodes D_{1-m} to initiate a selective discharge (selective eraser discharge).

[0010]

During this period, corresponding to the display data, all the discharge cells are grouped into the lighted cells in which eraser discharge is not caused to maintain the wall charge, and the non-lighted cells in which the eraser discharge is caused to erase the wall charge.

[0011]

In the sustain light-emission period I_c , sustain pulses IP_x , IP_y are applied between the row electrodes X_{1-n} , Y_{1-n} paired with each other at intervals corresponding to the weight of each sub-field, to thereby allow the sustain discharge to be repeatedly produced in only the lighted cells, having residual wall charge, at intervals in accordance with the intervals of application of the sustain pulses IP_x , IP_y .

[0012]

The discharge space between the front substrate and the back substrate is filled with a Ne-Xe gas containing 5 vol% xenon Xe. The sustain discharge allows radiation of 147nm-wavelength vacuum ultraviolet rays from xenon Xe.

[0013]

The vacuum ultraviolet rays excite the phosphor layers provided on the back substrate and then visible light is generated, resulting in the image display on the PDP.

[0014]

In the PDP as described above, although the reset discharge in the concurrent reset period R_c of the sub-field method generates priming particles (charged particles) in the discharge space of all the discharge cells, the priming particles decrease as time goes by. Hence, the priming particles decrease in the display lines (e.g. an n^{th} display line which forms the final scan line) in which the time interval until the next selection is operated (the scan pulses SP are applied) after the concurrent reset is operated is much longer than in the other display lines.

[0015]

For this reason, in such discharge cells having a less quantity of priming particles, the discharge delay time is extended or variations of the discharge delay time are increased. This causes the selective discharge operation in the addressing

period W_c to be unstable and to have a tendency to produce a false discharge, resulting in a disadvantage of loss of quality of displayed images.

[0016]

The present invention has been made to overcome the disadvantages associated with the conventional plasma display panel as described hereinbefore.

It is therefore an object of the present invention to provide a plasma display panel capable of preventing a false discharge to improve the quality of displayed images.

[0017]

[Means of Solving the Problems]

To attain the above object, a plasma display panel according to a first invention includes a front substrate and a back substrate on opposite sides of a discharge space; a plurality of row electrode pairs extending in a row direction and arranged in a column direction on the front substrate to form display lines; a protective dielectric layer provided on a face of the front substrate facing the discharge space; a plurality of column electrodes extending in the column direction and arranged in the row direction on the back substrate to form a unit light emitting area in the discharge space at each intersection with the row electrode pair; and a phosphor layer on a face of the back substrate facing the discharge space, and is characterized in that a secondary electron emissive layer, which is formed of a material having a coefficient of secondary electron emission higher than that of dielectrics forming said protective dielectric layer, is placed at a site facing each unit light emitting area between the front substrate and the back substrate.

[0018]

In the plasma display panel according to the first invention, reset pulses are concurrently applied between the

row electrodes paired with each other during a concurrent reset period. By this application, discharge is produced in all the unit light emitting areas in unison to form a predetermined amount of wall charge in each unit light emitting area.

[0019]

In the subsequent addressing period, scan pulses are sequentially applied to the row electrodes each of which is one of the row electrode pair, and display data pulses corresponding to the display data in each display line are applied to the column electrodes to initiate a selective discharge.

[0020]

During this period, corresponding to the display data, all the discharge cells are grouped into the lighted cells in which eraser discharge is not initiated to maintain the wall charge, and the non-lighted cells in which the eraser discharge is initiated to erase the wall charge.

[0021]

In the subsequent sustain light-emission period, sustain pulses are applied between the row electrodes paired with each other, to allow the sustain discharge to be produced in the lighted cells having residual wall charge, resulting in generation of an image.

[0022]

In the reset discharge when an image is generated, the visible light radiated from the phosphor layer provided in each unit light emitting area excites the material having a high coefficient of secondary electron emission (a small work function) and forming the secondary electron emissive layer, whereupon secondary electrons are emitted from the secondary electron emissive layer into the discharge space of the unit light emitting area.

[0023]

For this reason, even when dielectrics forming the

protective dielectric layer has a low coefficient of secondary electron emission, the amount of priming particles emitted into the discharge space is increased due to the provision of the secondary electron emissive layer, and the resulting secondary electrons serves for re-generating priming particles, which results in ensuring a sufficient amount of priming particle in the addressing period.

[0024]

According to the first invention as described above, the secondary electron emissive layer ensures a sufficient amount of priming particles during the addressing period. This inhibits an increase of a discharge delay time and also producing of variations of the discharge delay time in the display line in which a time interval until the scan pulses are applied in the subsequent addressing period after the concurrent reset period increases. The inhibitions lead to prevention of a selective discharge operation in the addressing period from becoming unstable to cause a false discharge, resulting in generation of high quality images.

[0025]

To attain the aforementioned object, a plasma display panel according to an second invention features, in addition to the configuration of the first invention, in that the secondary electron emissive layer extends in the row direction at each site opposing the row electrode pairs, and faces toward the discharge space of the unit light emitting areas adjacent to each other in the column direction. With this configuration, the secondary electrons are emitted from the secondary electron emissive layer into the discharge space in the unit light areas adjacent to the secondary electron emissive layer in the column direction, and the priming particles are re-generated in the unit light emitting area. Thus, a sufficient amount of priming particles is ensured in the unit light emitting area.

【0026】

To attain the aforementioned object, a plasma display panel according to a third invention features, in addition to the configuration of the first invention, in that the secondary electron emissive layer extends in the column direction at each site between the unit light emitting areas adjacent to each other in the row direction, and faces toward the discharge space of the unit light emitting areas adjacent to each other in the row direction. With this configuration, the secondary electrons are emitted from the secondary electron emissive layer into the discharge space in the unit light areas adjacent to the secondary electron emissive layer in the row direction, and the priming particles are re-generated in the unit light emitting area. Thus, a sufficient amount of priming particles is ensured in the unit light emitting area.

【0027】

To attain the aforementioned object, a plasma display panel according to a fourth invention features, in addition to the configuration of the first invention, in that a partition wall, which includes a transverse wall section extending in the row direction and a vertical wall section extending in the column direction and is disposed between the front substrate and the back substrate, partitions the discharge space into the unit light emitting areas, and the secondary electron emissive layer is provided between the front substrate and the transverse wall section of the partition wall. With this configuration, the secondary electrons are emitted from the secondary electron emissive layer into the discharge space in the unit light areas adjacent to the secondary electron emissive layer in the column direction, and the priming particles are re-generated in the unit light emitting area. Thus, a sufficient amount of priming particles is ensured in the unit light emitting area.

【0028】

To attain the aforementioned object, a plasma display panel according to a fifth invention features, in addition to the configuration of the first invention, in that a partition wall, which includes a transverse wall section extending in the row direction and a vertical wall section extending in the column direction and is disposed between the front substrate and the back substrate, partitions the discharge space into the unit light emitting areas, and the secondary electron emissive layer is provided between the front substrate and the vertical wall section of the partition wall. With this configuration, the secondary electrons are emitted from the secondary electron emissive layer into the discharge space in the unit light areas adjacent to the secondary electron emissive layer in the row direction, and the priming particles are re-generated in the unit light emitting area. Thus, a sufficient amount of priming particles is ensured in the unit light emitting area.

[0029]

To attain the aforementioned object, a plasma display panel according to a sixth invention features, in addition to the configuration of the first invention, in that a stripe-patterned partition wall is disposed between the front substrate and the back substrate and extends in the column direction for partitioning the discharge space into the unit light emitting areas aligned in the column direction, and the secondary electron emission layer extends in the row direction at a site opposing main bodies of the row electrodes. With this configuration, the secondary electrons are emitted from the secondary electron emissive layer into the discharge space in the unit light areas adjacent to the secondary electron emissive layer in the column direction, and the priming particles are re-generated in the unit light emitting area. Thus, a sufficient amount of priming particles is ensured in the unit light emitting area.

[0030]

To attain the aforementioned object, a plasma display panel according to a seventh invention features, in addition to the configuration of the first invention, in that the phosphor layer contains the material, having a coefficient of secondary electron emission higher than that of the dielectrics forming the protective dielectric layer, to be formed in combination with the secondary electron emissive layer. With this configuration, the secondary electrons are emitted from the phosphor layer into the discharge space in the unit light areas, which is accompanied with the discharge. Thus, a sufficient amount of priming particles is ensured in the unit light emitting area.

[0031]

To attain the aforementioned object, a plasma display panel according to an eighth invention features, in addition to the configuration of the first invention, in that an ultraviolet region light emissive layer, which is formed of an ultraviolet region light emitting phosphor having persistence characteristics allowing continuous radiation of ultraviolet light as a result of excitation by ultraviolet rays having a predetermined wavelength, or a visible region light emissive layer, which is formed of a visible region light emitting phosphor having persistence characteristics allowing continuous radiation of visible light as a result of excitation by ultraviolet rays having a predetermined wavelength, are placed at a site facing each unit light emitting area between the front substrate and the back substrate.

[0032]

According to the plasma display panel of the eighth invention, in the reset discharge when an image is generated, ultraviolet rays radiated from the discharge gas filled into the discharge space excite an ultraviolet region light emissive

layer or a visible region light emissive layer, whereupon ultraviolet light or visible light is radiated.

[0033]

The ultraviolet region light emissive layer or the visible region light emissive layer continues radiating the ultraviolet light or the visible light due to the persistence characteristics of the ultraviolet region light emitting phosphor forming the ultraviolet region light emissive layer or of the visible region light emitting phosphor forming the visible region light emissive layer. Hence, during the addressing period, secondary electrons are emitted from the protective dielectric layer or the secondary electron emissive layer by the ultraviolet light or the visible light, then priming particles are re-generated in the discharge space in the unit light emitting areas. A reduction of the amount of priming particles in each unit light emitting area is thus inhibited, leading to inhibition of an increase of the discharge delay time and producing of variations of the discharge delay time.

[0034]

To attain the aforementioned object, a plasma display panel according to a ninth invention features, in addition to the configuration of the eighth invention, in that the phosphor layer contains the ultraviolet region light emitting phosphor or the visible region light emitting phosphor to be formed in combination with the ultraviolet region light emissive layer or the visible region light emitting phosphor layer.

[0035]

With the above configuration, the phosphor layer has the persistence characteristics. Ultraviolet light or visible light is continuously emitted from the ultraviolet region light emitting phosphor or visible region light emitting phosphor which is contained in the phosphor layer so that the priming

particles are re-generated. This inhibits a reduction of the amount of priming particles in each unit light emitting area.

[0036]

To attain the aforementioned object, a plasma display panel according to a tenth invention features, in addition to the configuration of the eighth invention, in that the ultraviolet region light emitting phosphor forming the ultraviolet region light emissive layer or the visible region light emitting phosphor forming the visible region light emissive layer is a light emissive material having persistence characteristics allowing radiation for 0.1 msec or more. With this configuration, it is possible to re-generate the priming particles after completing the concurrent reset period and during the following addressing period to inhibit a reduction in the amount of priming particles in each unit light emitting area.

[0037]

To attain the aforementioned object, a plasma display panel according to an eleventh invention features, in addition to the configuration of the first invention, in that the secondary electron emissive layer contains an ultraviolet region light emitting phosphor having persistence characteristics allowing continuous radiation of ultraviolet light as a result of excitation by ultraviolet rays having a predetermined wavelength, or a visible region light emitting phosphor having persistence characteristics allowing continuous radiation of visible light.

[0038]

With the above configuration, the secondary electron emissive layer itself has the persistence characteristics. Ultraviolet light or visible light is continuously emitted from the ultraviolet region light emitting phosphor or visible region light emitting phosphor which is contained in the

secondary electron emissive layer so that the priming particles are re-generated. This inhibits a reduction of the amount of priming particles in each unit light emitting area.

[0039]

To attain the aforementioned object, a plasma display panel according to a twelfth invention features, in addition to the configuration of the first invention, in that the phosphor layer is formed of a light emissive material having persistence characteristics allowing radiation for 0.1 msec or more. With this configuration, visible light is continuously emitted from the phosphor layer itself during the addressing period so that the priming particles are re-generated. Thus, a reduction in the amount of priming particles in each unit light emitting area is inhibited.

[0040]

To attain the aforementioned object, a plasma display panel according to a thirteenth invention features, in addition to the configuration of the eighth invention, in that a light absorption layer is provided at each position opposing a non-lighting area between the unit light emitting areas adjacent to each other in the row direction or the column direction of the front substrate, and opposite the back substrate in relation to the ultraviolet region light emissive layer or visible region light emissive layer. This design prevents the reflection of ambient light, incident through the front substrate, on the non-lighting area in the screen, to improve the contrast on the display screen.

[0041]

[Preferred embodiments of the invention]

Most preferred embodiment according to the present invention will be described hereinafter in detail with reference to the accompanying drawings.

[0042]

Figs. 1 to 6 illustrate a first example of an embodiment of a plasma display panel (hereinafter referred to as "PDP") according to the present invention. Fig. 1 is a front view schematically illustrating the PDP in the first example. Fig. 2 is a section view taken along the V1-V1 line of Fig. 1. Fig. 3 is a section view taken along the V2-V2 line of Fig. 1. Fig. 4 is a section view taken along the W1-W1 line of Fig. 1. Fig. 5 is a section view taken along the W2-W2 line of Fig. 1. Fig. 6 is a section view taken along the W3-W3 line of Fig. 1.

[0043]

In the PDP illustrated in Figs. 1 to 6, a plurality of row electrode pairs (X, Y) are arranged in parallel on a back face of a front glass substrate 10 serving as a display surface and extend in a row direction (the right-left direction in Fig. 1) of the front glass substrate 10.

[0044]

The row electrode X is made up of transparent electrodes Xa formed in a T-like shape of a transparent conductive film made of ITO or the like, and a bus electrode Xb which is formed of metal film extending in the row direction of the front glass substrate 10 and connects to a narrowed proximal end of each transparent electrode Xa.

[0045]

Likewise, the row electrode Y made up of transparent electrodes Ya formed in a T-like shape of a transparent conductive film made of ITO or the like, and a bus electrode Yb which is formed of a metal film extending in the row direction of the front glass substrate 10 and connects to a narrowed proximal end of each transparent electrode Ya.

[0046]

The row electrodes X and Y are alternately disposed in a column direction of the front glass substrate 10 (in the vertical direction in Fig. 1). The transparent electrodes Xa

and Ya arranged along the respective bus electrodes Xb and Yb extend toward the row electrode as the pair to each other such that the top sides of the widened portions of the transparent electrodes Xa and Ya oppose each other on the opposite sides of a discharge gap g having a predetermined width.

[0047]

Each of the bus electrodes Xb, Yb is formed in a double-layer structure with a black conductive layer Xb', Yb' on the display surface side and a main conductive layer Xb'', Yb'' on the back substrate side.

[0048]

On the back face of the front glass substrate 10 and between the back-to-back bus electrodes Xb and Yb of the respective row electrode pairs (X, Y) adjacent to each other in the column direction, a black light absorption layer (light-shield layer) 30 extends along the bus electrodes Xb, Yb in the row direction. Additionally, a light absorption layer (light-shield layer) 31 is provided at a position opposing a vertical wall 35a of a partition wall 35.

[0049]

On the back face of the front glass substrate 10, further, a dielectric layer 11 overlays the row electrode pairs (X, Y). On the back face of the dielectric layer 11, an additional dielectric layer 11A juts out of the back face of the dielectric layer 11 at a position opposing the adjacent bus electrodes Xb and Yb of the respective row electrode pairs (X, Y) adjacent to each other, and opposing an area between the adjacent bus electrodes Xb and Yb, and extends in parallel to the bus electrodes Xb, Yb.

[0050]

On the back faces of the dielectric layer 11 and the additional dielectric layers 11A, a protective layer (protective dielectric layer) 12 made of MgO is provided.

[0051]

Next, a back glass substrate 13 is disposed in parallel to the front glass substrate 10. On the front face of the back glass substrate 13 on the display surface side, column electrodes D are arranged in parallel at regularly established intervals from each other and extend in the direction perpendicular to the row electrode pairs (X, Y) (in the column direction), at positions opposing the paired transparent electrodes Xa and Ya of each row electrode pair (X, Y).

[0052]

A white dielectric layer 14 is further provided on the front face of the back glass substrate 13 on the display surface side, and the partition wall 35 is provided on the dielectric layer 14.

[0053]

The partition wall 35 is formed in a ladder pattern by vertical walls 35a extending in the column direction between the adjacent column electrodes D disposed in parallel to each other, and transverse walls 35b extending in the row direction at positions opposing the additional dielectric layers 11A.

[0054]

The ladder-patterned partition wall 35 defines the space between the front glass substrate 10 and the back glass substrate 13 into each portion facing the paired transparent electrodes Xa and Ya of each row electrode pair (X, Y) to form quadrangular discharge spaces S.

[0055]

The face of the vertical wall 35a of the partition wall 35 on the display surface side is out of contact with the protective layer 12 (see Figs. 3 and 4) to form a clearance α therebetween. The face of the transverse wall 35b on the display surface side is also out of direct contact with the portion of the protective layer 12 which overlays the additional

dielectric layer 11A (see Figs. 2, 3 and 5).

[0056]

On the five faces of a front face of the dielectric layer 14 and side faces of the vertical walls 35a and transverse walls 35b of the partition wall 35 which face the discharge space S, a phosphor layer 16 overlays all the five faces in each discharge space S.

[0057]

The phosphor layers 16 are set in order of red (R), green (G) and blue (B) for the sequence of discharge spaces S in the row direction (see Fig. 4).

[0058]

The inside of the discharge space S is filled with a discharge gas containing xenon Xe.

[0059]

A transverse wall 35b of a ladder-patterned partition wall 35 which defines the discharge spaces S is separated from a transverse wall 35b of an adjacent partition wall 35 in the column direction by an interstice SL provided at a location overlapping the light absorption layer 30 between the display lines.

[0060]

In other words, each of the ladder-patterned partition walls 35 extends along the direction of the display line (row) L, and are disposed in parallel to each other in the column direction on opposite sides of the interstice SL extending along the discharge line L.

[0061]

A width of each transverse wall 35b is set to be approximately equal to a width of each vertical wall 35a.

[0062]

For the PDP, as illustrated in Figs. 2, 3 and 6, a secondary electron emissive layer 17 is further provided at a portion on

the back face of the protective layer 12 opposing a face of the transverse wall 35b of each partition wall 35 on the display surface side. The secondary electron emissive layer 17 includes a material having a higher coefficient of secondary electron emission (a smaller work function) than that of MgO making up a protective layer 12 which overlays a dielectric layer 11 and an additional dielectric layer 11A. The secondary electron emissive layer 17 is in contact with the face of a transverse wall 19b on the display surface side while facing toward the interior of the discharge space S to shield each discharge space S from an interstice SL.

[0063]

It should be mentioned that the secondary electron emissive layer 17 may be provided on the face of the transverse wall 35b of the partition wall 35 on the display surface side.

[0064]

The reason of providing the secondary electron emissive layer 17 is as follows.

[0065]

The protective layer 12 made of MgO serves a facility to protect the dielectric layer 11 and the additional dielectric layer 11A from the impact of ions, and a facility to emit secondary electrons into the discharge space S by the discharge to generate priming particles. MgO has a relatively large work function (a discharge voltage required for emitting secondary electrons) of approximate 4.2 eV, and therefore the emission of secondary electrons is difficult. For this reason, by providing the secondary electron emissive layer 37 made of the material having a higher coefficient of secondary electron emission (a smaller work function) than that of MgO, the amount of secondary electrons emitted into the discharge space S is increased.

[0066]

Examples of the material having a high coefficient of secondary electron emission and insulation properties for forming the secondary electron emissive layer 17, include oxides of alkali metals (e.g. Cs_2O), oxides of alkali-earth metals (e.g. CaO , SrO , BaO), fluorides (CaF_2 , MgF_2), and the like.

[0067]

At this point, these materials have a higher coefficient of secondary electron emission than that of MgO but a smaller strength for the impact of ions than that of MgO . Accordingly, since the materials are inferior in terms of protection for the dielectric layer 11, it is preferable to provide the protective layer 12 independently.

The secondary electron emissive layer 17 may be formed of materials of which a coefficient of secondary electron emission is increased as a result of the introduction of impurity level into crystals caused by crystal defects or impurities.

[0068]

For example, the secondary electron emissive layer 17 can be formed of a material of which a coefficient of secondary electron emission is increased by means of changing the composition ratio into 1:1 as MgOx to introduce crystal defects.

[0069]

In the above-mentioned PDP, each row electrode pair (X, Y) forms a display line (row) L on the matrix display screen. Each discharge space S defined by the ladder-patterned partition wall 35 defines a discharge cell C.

[0070]

Images are displayed on the PDP by the sub-field method as in the case having been discussed in Fig. 12.

[0071]

Specifically, after the concurrent reset, the selective

discharge is operated between the row electrode pair (X, Y) and the column electrode D in each discharge cell through the addressing operation. This scatters the lighted cells (the discharge cells C in which the wall charge is formed on the dielectric layer 11) and the non-lighted cells (the discharge cells C in which the wall charge is not formed on the dielectric layer 11) in all the display lines L throughout the panel in accordance with the image to be displayed.

[0072]

After the addressing operation, in all the display lines L, discharge sustain pulses are applied alternatively to the row electrode pairs (X, Y) at intervals corresponding to the weight of each sub-field in unison. A surface discharge is initiated in each lighted cell in every application of the discharge sustain pulse to generate ultraviolet light. By the generated ultraviolet light, each R, G, B phosphor layer 16 in the discharge space S is excited to emit light, resulting in generating a display screen.

[0073]

The images are generated on the PDP as described above. In the reset discharge when the image is generated, the visible light radiated from the R, G or B phosphor layer 16 in each discharge cell C excites the material having a high coefficient of secondary electron emission (a small work function) and making up the secondary electron emissive layer 17, to allow the secondary electron emissive layer 17 to emit secondary electrons into the discharge cell.

[0074]

At this time, the phosphor layers 16 painted red R ((Y, Gd)BO₃:Eu) and green G (Zn₂SiO₄:Mn) continue emitting the visible light for more than several milliseconds by the reset discharge. Due to the emitted visible light, the secondary electron emissive layer 17 emits the secondary electrons during

the addressing period W_c in one sub-field (see Fig. 12). Due to the emitted secondary electrons, priming particles are regenerated, resulting in inhibiting a reduction of the amount of priming particles in the discharge cell C.

[0075]

Thus, by inhibiting the reduction of the amount of priming particles, an increase of a discharge delay time in the addressing period W_c is inhibited, and also producing variations of the discharge delay time is inhibited. Therefore, even when a pulse width of the scan pulse SP (see Fig. 12) and the display data pulse are narrow, it is prevented that the selective discharge operation in the addressing period W_c becomes unstable to produce a false discharge. This allows the generation of images with high quality and a reduction of the time of the addressing period.

[0076]

The graph (A) in Fig. 7 shows the results of measurement of a discharge delay time and variations of discharge light emission using an oscillograph in the above PDP, where F is the discharge light emission, T_1 is the discharge delay time and F_u is the variation of discharge light emission.

[0077]

From a comparison between the graph (A) in Fig. 7 and the graph (B) in Fig. 7 shows a discharge delay time T_1' and variations of discharge light emission F_u' where the secondary electron emissive layer 17, it is seen that both the discharge delay time and the variation of discharge light emission decrease.

[0078]

In the examples of Figs. 1 to 6, the secondary electron emissive layer 17 is disposed only between the face of the protective layer 12 on the back substrate side and the face of the transverse wall 35b of the partition wall 35 on the display

surface side. However, as illustrated in Fig. 8, a secondary electron emissive layer 17' may be provided on the face of the vertical wall 35a of the partition wall 35 on the display surface side. Alternatively, the secondary electron emissive layer 17' may be provided on the protective layer 12 on the back substrate side opposing the vertical wall 35a so as to be disposed at a site facing toward the interior of the discharge space of each discharge cell C between the vertical wall 35a and the protective layer 12.

[0079]

This increases an area of the secondary electron emissive layer 17' in contact with the discharge space of the discharge cells C to increase the amount of emission of secondary electrons, and therefore a sufficient amount of priming particles in the addressing period W_c in one sub-field can be ensured.

[0080]

In the above example, the phosphor layer 16 may include a material having a high coefficient of secondary electron emission (a small work function) to serve also as the secondary electron emissive layer.

[0081]

The secondary electron emissive layer may be coated on the inner wall-face of the partition wall 35, or coated on the protective layer 12 on the front glass substrate 10 side.

[0082]

In the PDP of each example described hereinbefore, a light emissive layer can face toward the interior of the discharge space in each discharge cell C in order to increase secondary electrons emitted from the protective layer 12 and secondary electron emissive layer 17, or the phosphor layer 16 containing the material having a high coefficient of secondary electron emission, resulting from radiation of excitation light which

excites the material of a high coefficient of secondary electron emission

As a type of such a light emissive layer, there are an ultraviolet region light emissive layer and a visible region light emissive layer.

[0083]

The ultraviolet region light emissive layer is made of ultraviolet region light emitting phosphor having the persistence characteristics allowing continuous emission of ultraviolet light for 0.1 msec or more, preferably, 1 msec or more (i.e. approximate length of time of the addressing period W_c) resulting from excitation by 147nm-wavelength vacuum ultraviolet rays which are radiated by a discharge from xenon Xe included in a discharge gas filled in the discharge space S.

[0084]

Examples of the ultraviolet region light-emitting phosphor having such persistence characteristics, include $BaSi_2O_3:Pb^{2+}$ (a wavelength of emitted light: 350 nm), $SrB_4O_7F:Eu^{2+}$ (wavelength of emitted light: 360 nm), $(Ba, Mg, Zn)_2Si_2O_7:Pb^{2+}$ (wavelength of emitted light: 295 nm), $YF_3:Gd, Pr$, and so on.

[0085]

The visible region light emissive layer is made of visible region light emitting phosphor having the persistence characteristics allowing continuous radiation of ultraviolet light for 0.1 msec or more, preferably, 1 msec or more (i.e. approximate length of time of the addressing period W_c) resulting from excitation by 147nm-wavelength vacuum ultraviolet rays radiated from xenon Xe by the discharge.

[0086]

Examples of the visible region light emissive layer having such persistence characteristics, are phosphor materials such as red R ($(Y, Gd)Bo_3:Eu$) and green G ($Zn_2SiO_4:Mn$),

and the like.

[0087]

The ultraviolet region light emissive layer and the visible region light emissive layer are excited by 147nm-wavelength vacuum ultraviolet rays radiated from xenon Xe in the discharge gas by the discharge, and thus radiate ultraviolet light.

[0088]

The ultraviolet light emitted from the ultraviolet region light emissive layer or the visible region emissive layer allows secondary electrons to be emitted from the protective layer (MgO layer) 12 and the secondary electron emissive layer 17 or the phosphor layer 16 including the material having a high coefficient of secondary electron emission, and thus priming particles are continuously regenerated in the discharge space of the discharge cell C during the addressing period W_c in one sub-field (see Fig. 12). This inhibits a reduction of the amount of priming particles in each lighted cell.

[0089]

Accordingly, the ultraviolet light radiated from the ultraviolet region light emissive layer or the visible region light emissive layer, increases the amount of secondary electron emission, to further inhibit the reduction of the amount of priming particles in the lighted cell. This further inhibits the extension of a discharge delay time in the addressing period W_c , and the producing of variations of the discharge delay time.

[0090]

It is possible to provide the ultraviolet region light emissive layer and the visible region light emissive layer, aside from the secondary electron emissive layer 17, at a site facing toward the discharge space in a clearance between the front glass substrate 10 and the partition wall 35. However,

the ultraviolet region light emissive layer or the visible region light emissive layer may contain the material having a high coefficient of secondary electron emission (a small work function), to be formed in combination with the secondary electron emissive layer 17.

[0091]

Alternatively, the ultraviolet region light emissive layer or the visible region light emissive layer together with a material having a high coefficient of secondary electron emission (small work function) can be contained in the phosphor layer 16.

[0092]

The PDP is constructed such that the transverse walls 35b of the respective partition walls 35 adjacent to each other in the column direction are spaced from each other by the interstice SL extending in the row direction, and a width of each transverse wall 35b is approximately equal to a width of each vertical wall 35a. For this reason, the front glass substrate 10 and the back glass substrate 13 may not produce warpage when the partition wall 35 is burned, and the shape of the discharge cell may be not deformed by damage to the partition wall 35, or the like.

[0093]

In the PDP, portions of the back face of the front glass substrate 10 except for portions thereof facing the discharge spaces S are covered with the light absorption layers 30, 31 and the black conductive layers Xb', Yb' of the bus electrodes Xb, Yb formed in the double-layer structure. This allows prevention of the reflection of ambient light incident through the front glass substrate 10 and the associated enhancement of contrast on the display screen.

[0094]

It should be noted that in the first example, any one of

the light absorption layers 30 and 31 may be provided.

Further, a color filter layer (not shown) having colors corresponding to the colors (R, G, B) of each phosphor layer 16 in the discharge space S facing the color filter layer can be provided on the back face of the front glass substrate 10 in each discharge cell C.

[0095]

In this case, the light absorption layers 30, 31 are provided in a space between the color filter layers, formed in an island pattern and facing each discharge space S, or on a position corresponding to the space.

[0096]

Figs. 9 to 11 illustrate a second example of the embodiment of PDP according to the present invention. Fig. 9 is a plan view schematically illustrating the PDP in the second example. Fig. 10 is a section view taken along the V3-V3 line in Fig. 9. Fig. 11 is a section view taken along the W4-W4 line in Fig. 9.

[0097]

In the foregoing first example, the vertical walls and the transverse walls of the partition wall surround the discharge cell at all directions for definition. In contrast, the PDP illustrated in Figs. 9 to 11 is configured such that a stripe-patterned partition wall 45 extending in the column direction defines a discharge space S between a front glass substrate 10 and a back glass substrate 13.

[0098]

The remaining configuration of the PDP is similar to the PDP in the first example except for the shape of transparent electrodes X1a, Y1a of row electrode X1, Y1, and no provision of the additional dielectric layer in a dielectric layer 11. Bus electrode X1b, Y1b of the row electrode X1, Y1 is formed in a double-layer structure of a black conductive layer X1b',

Y1b' situated on the display surface side and a main conductive layer X1b'', Y1b'' situated on the back substrate side. On the back face of the front glass substrate 10, a black light absorption layer (light shield layer) 30 extends in the row direction along the bus electrode X1b, Y1b between the back-to-back bus electrodes X1b and Y1b of the respective row electrode pairs (X1, Y1) adjacent to each other in the column direction.

[0099]

At a portion of a dielectric layer 11' on the back substrate side opposing back-to-back bus electrodes X1b and Y1b and the light absorption layer 30 provided between the back-to-back bus electrodes X1b and Y1b, a secondary electron emissive layer 27 extends in the row direction and faces toward the discharge space S'.

[0100]

In this example, as in the first example, in a reset discharge when an image is generated, the visible light radiated from a phosphor layer 16' in each discharge cell excites a material having a high coefficient of secondary electron emission (a small work function) making up the secondary electron emissive layer 27, to cause secondary electrons to be emitted from the secondary electron emissive layer 27 into the discharge space S' of each discharge cell.

[0101]

In this way, in addition to secondary electrons emitted from a protective layer 12', secondary electrons are emitted also from the secondary electron emissive layer 27, and thus the amount of priming particles in the discharge space S' is ensured sufficiently. For this reason, an increase of a discharge delay time in the addressing period and producing variations of the discharge delay time are further inhibited.

[0102]

In the fourth example, the secondary electron emissive layer may be provided on a portion of the face of the stripe-patterned partition wall 45 on the display surface side so as to face the discharge space S'.

[0103]

As in the first example, in this example, an ultraviolet region light emissive layer or a visible region light emissive layer can be provided.

[0104]

Although the PDP in the second example does not provide the partition wall for defining each discharge cell C' in the column direction, the transparent electrodes X1a, Y1a of the respective row electrodes X1, Y1 protrude from the respective bus electrodes X1b, Y1b in the column direction to oppose each other, thereby suppressing interference between discharges in the adjacent discharge cells C' in the column direction.

[Brief Explanation of the Drawings]

[Figure 1]

Fig. 1 is a front view schematically illustrating a first example according to the present invention.

[Figure 2]

Fig. 2 is a section view taken along the V1-V1 line of Fig. 1.

[Figure 3]

Fig. 3 is a section view taken along the V2-V2 line of Fig. 1.

[Figure 4]

Fig. 4 is a section view taken along the W1-W1 line of Fig. 1.

[Figure 5]

Fig. 5 is a section view taken along the W2-W2 line of Fig. 1.

[Figure 6]

Fig. 6 is a section view taken along the W3-W3 line of Fig. 1.

[Figure 7]

Figs. 7 are graphs illustrating a discharge delay time and variations of the discharge delay time in the example.

[Figure 8]

Fig. 8 is a plan view illustrating another example of a secondary electron emissive layer.

[Figure 9]

Fig. 9 is a front view schematically illustrating a second example according to the present invention.

[Figure 10]

Fig. 10 is a section view taken along the V3-V3 line of Fig. 9.

[Figure 11]

Fig. 11 is a section view taken along the W4-W4 line of Fig. 9.

[Figure 12]

Fig. 12 is a time chart showing a sub-field method in a plasma display panel.

[Explanation of Codes]

10	... FRONT GLASS SUBSTRATE (FRONT SUBSTRATE).
11	... DIELECTRIC LAYER
11A	... ADDITIONAL DIELECTRIC LAYER
12	... PROTECTIVE LAYER (PROTECTIVE DIELECTRIC LAYER)
13	... BACK GLASS SUBSTRATE (BACK SUBSTRATE)
14	... DIELECTRIC LAYER
16	... PHOSPHOR LAYER
17, 17', 27	... SECONDARY ELECTRON EMISSIVE LAYER
30	... LIGHT ABSORPTION LAYER
31	... LIGHT ABSORPTION LAYER
35	... PARTITION WALL
35a	... VERTICAL WALL (VERTICAL WALL SECTION)

35b	... TRANSVERSE WALL (TRANSVERSE WALL SECTION)
45	... PARTITION WALL
X, X1	... ROW ELECTRODE
Y, Y1	... ROW ELECTRODE
Xa, X1a	... TRANSPARENT ELECTRODE
Ya, Y1a	... TRANSPARENT ELECTRODE
Xb, X1b	... BUS ELECTRODE (MAIN BODY)
Yb, Y1b	... BUS ELECTRODE (MAIN BODY)
Xb', Yb'	... BLACK LAYER (LIGHT ABSORPTION LAYER)
Xb'', Yb''	... WHITE LAYER (LIGHT REFLECTION LAYER)
D	... COLUMN ELECTRODE
S, S'	... DISCHARGE SPACE
SL	... INTERSTICE
C, C'	... DISCHARGE CELL (UNIT LIGHT EMITTING AREA)
L	... DISPLAY LINE
g	... GAP
r	... CLEARANCE
T1	... DISCHARGE TIME DELAY
F	... DISCHARGE LIGHT EMISSION
Fu	... VARIATION OF DISCHARGE LIGHT EMISSION

$V_1 \rightarrow V_2 \rightarrow$

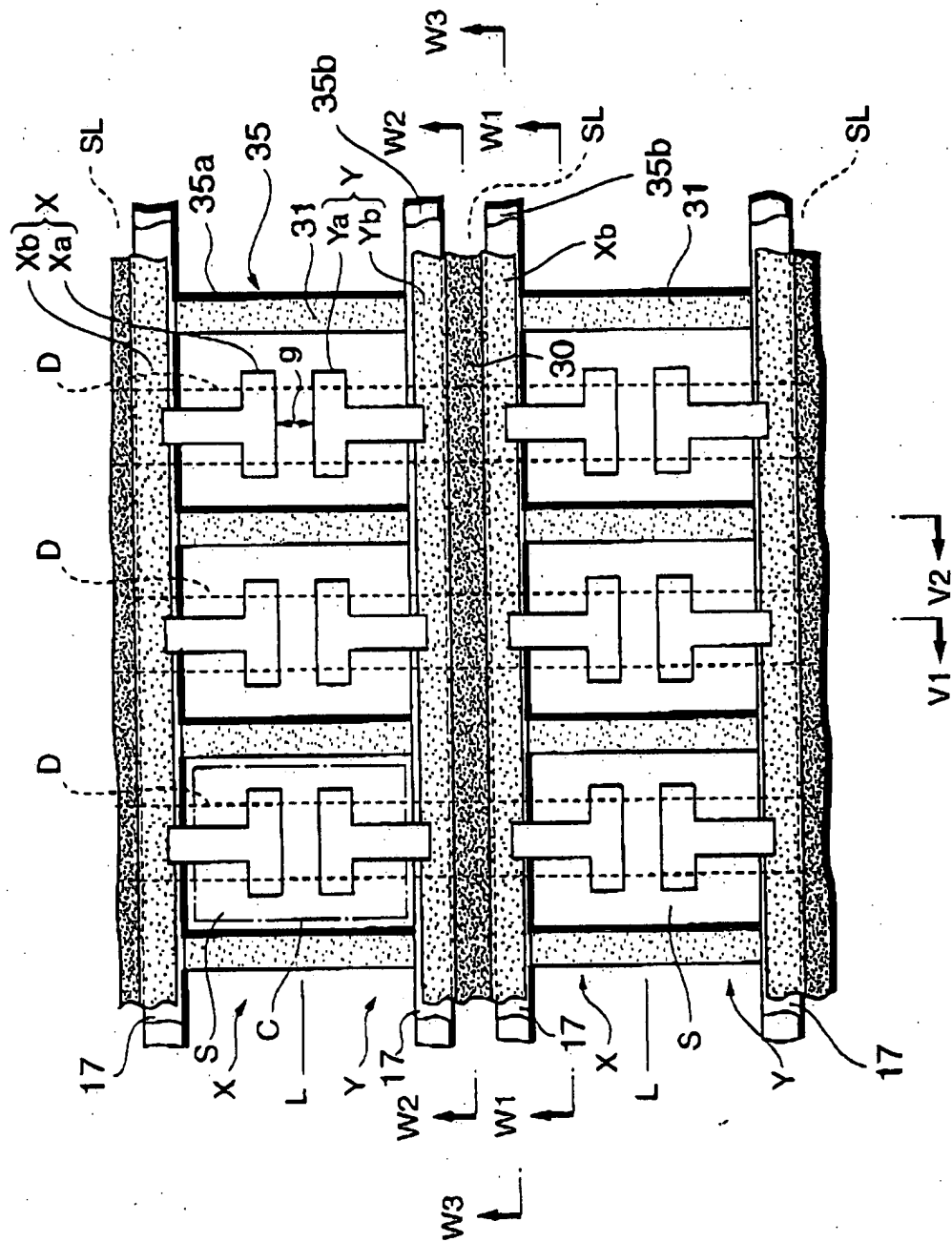


FIG.2

SECTION V1-V1

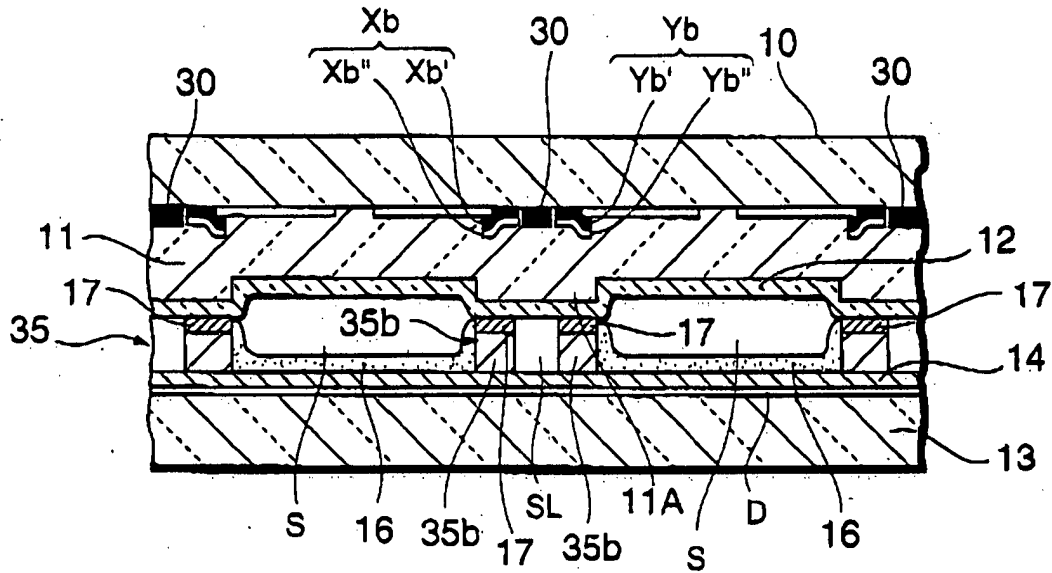


FIG.3

SECTION V2-V2

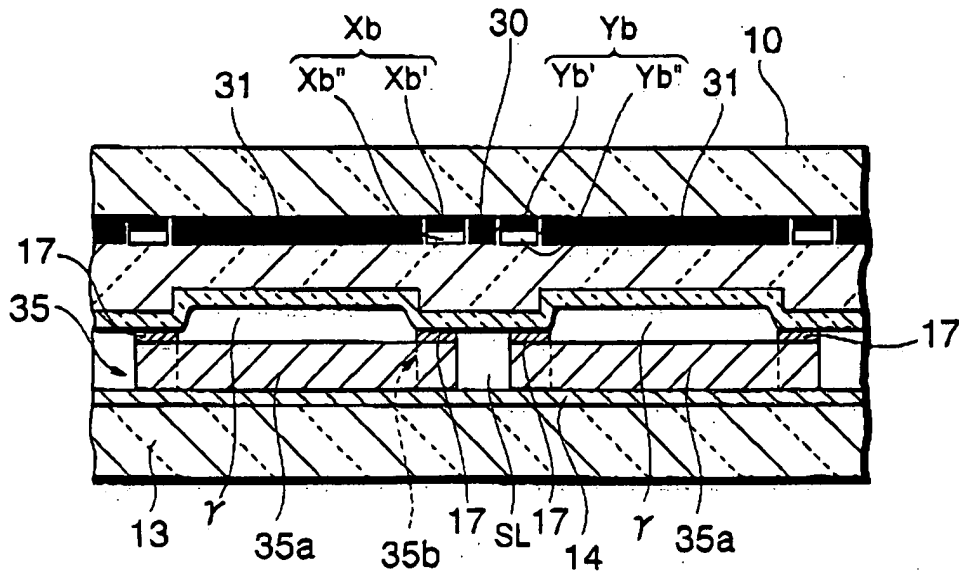


FIG.4

SECTION W1-W1

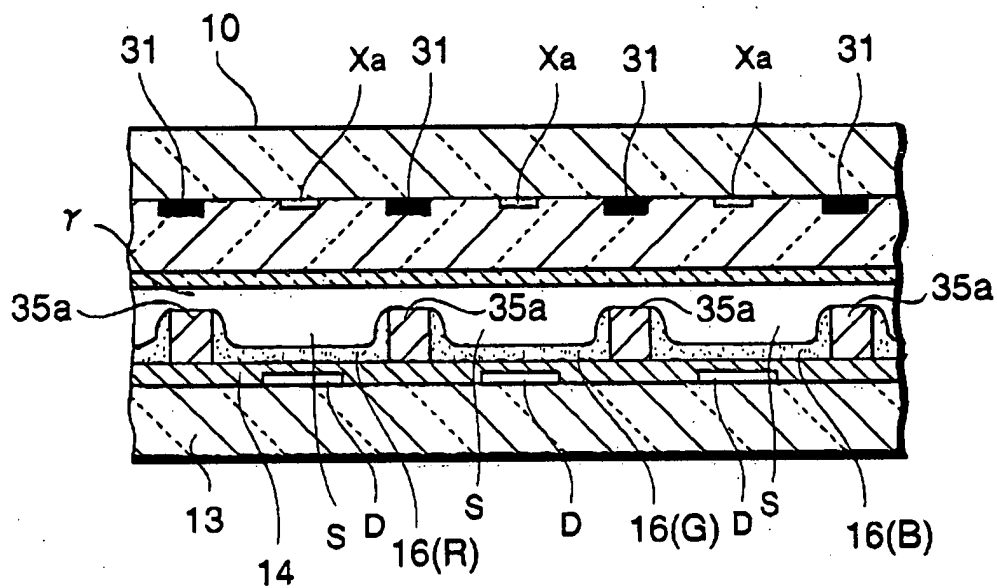


FIG.5

SECTION W2-W2

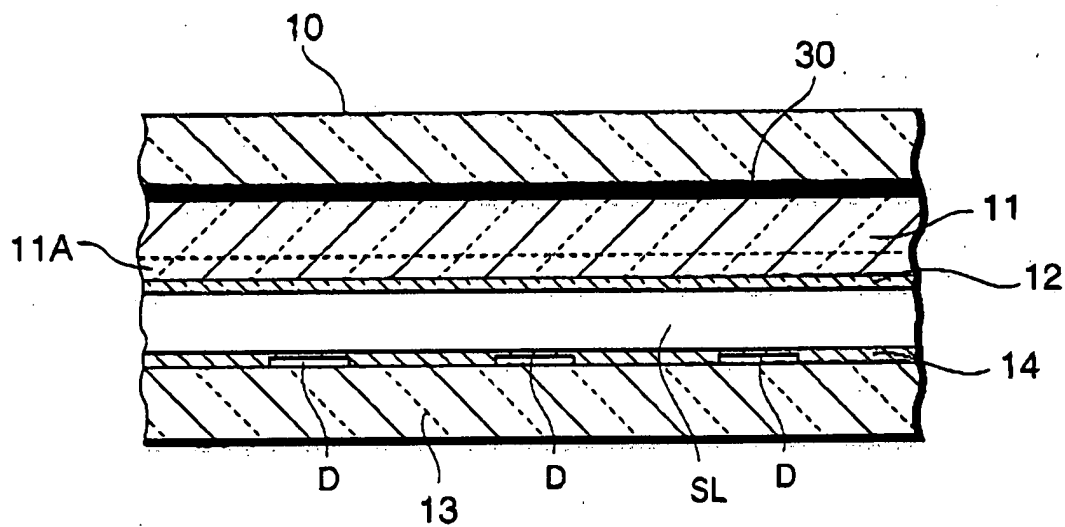


FIG.6

SECTION W3—W3

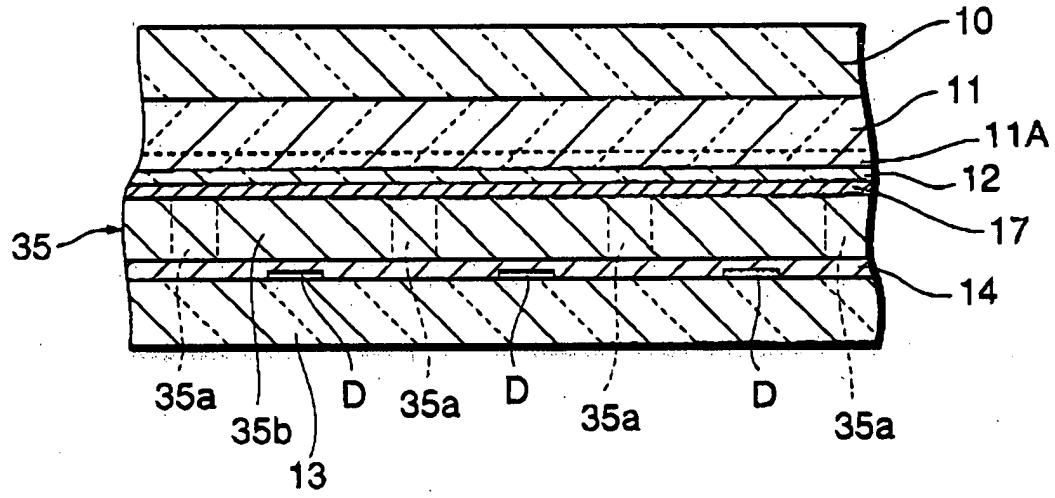
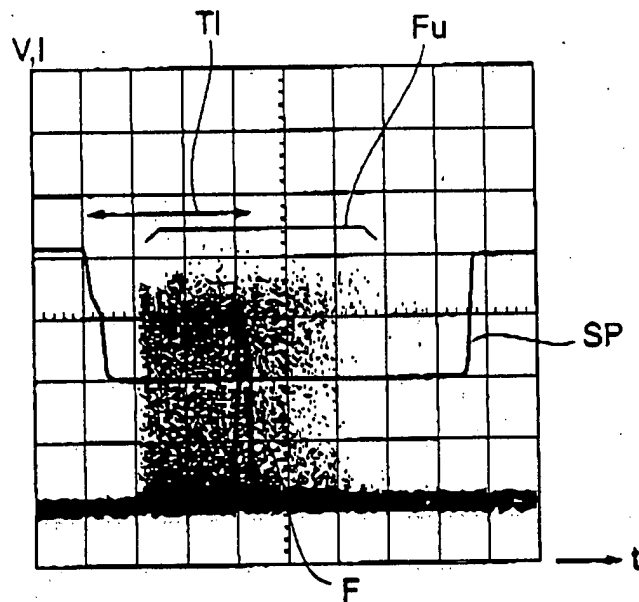


FIG.7

(A)WITH ULTRAVIOLET REGION LIGHT EMISSIVE LAYER



(B)WITHOUT ULTRAVIOLET REGION LIGHT EMISSIVE LAYER

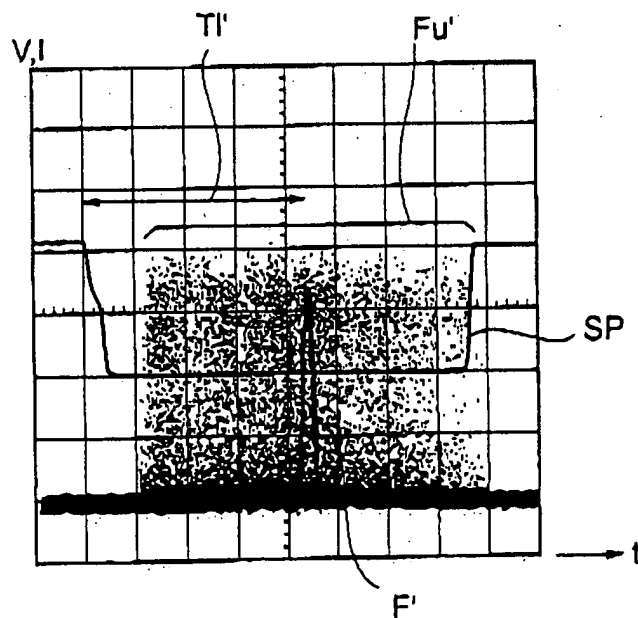


FIG. 8

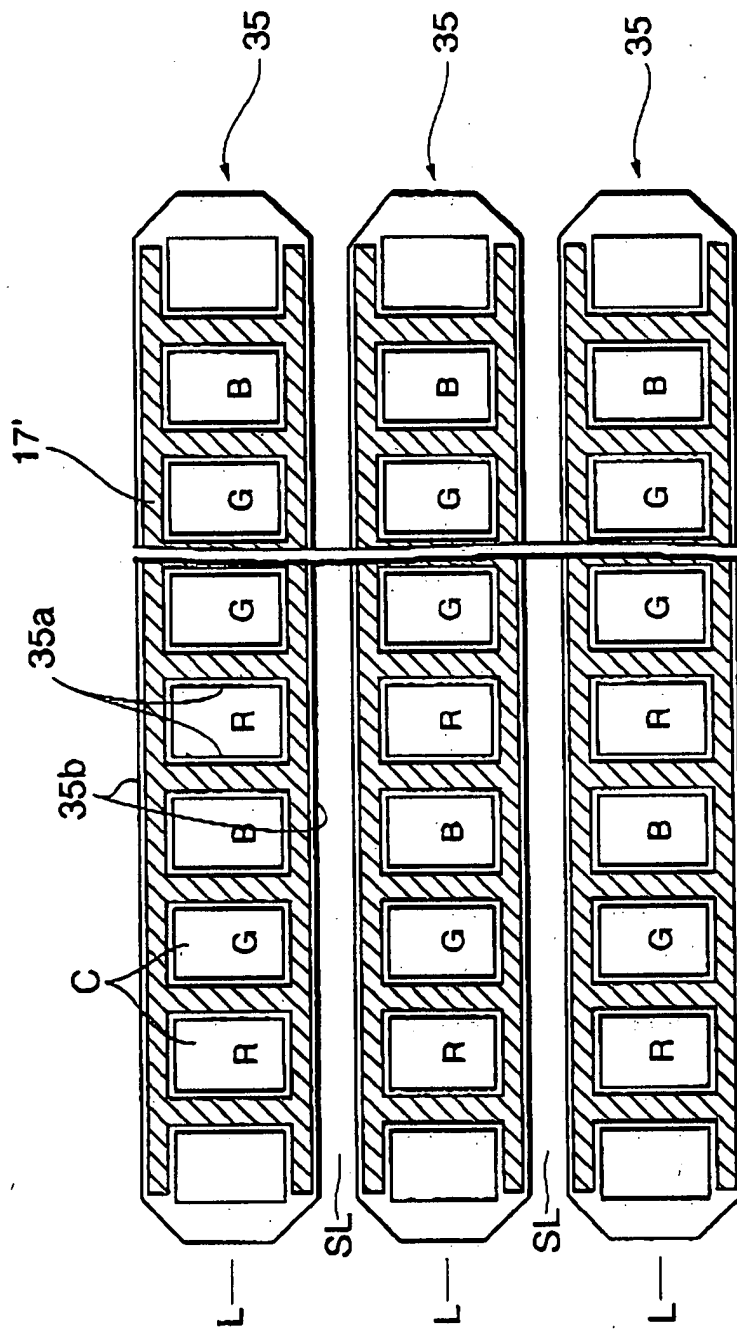


FIG. 9

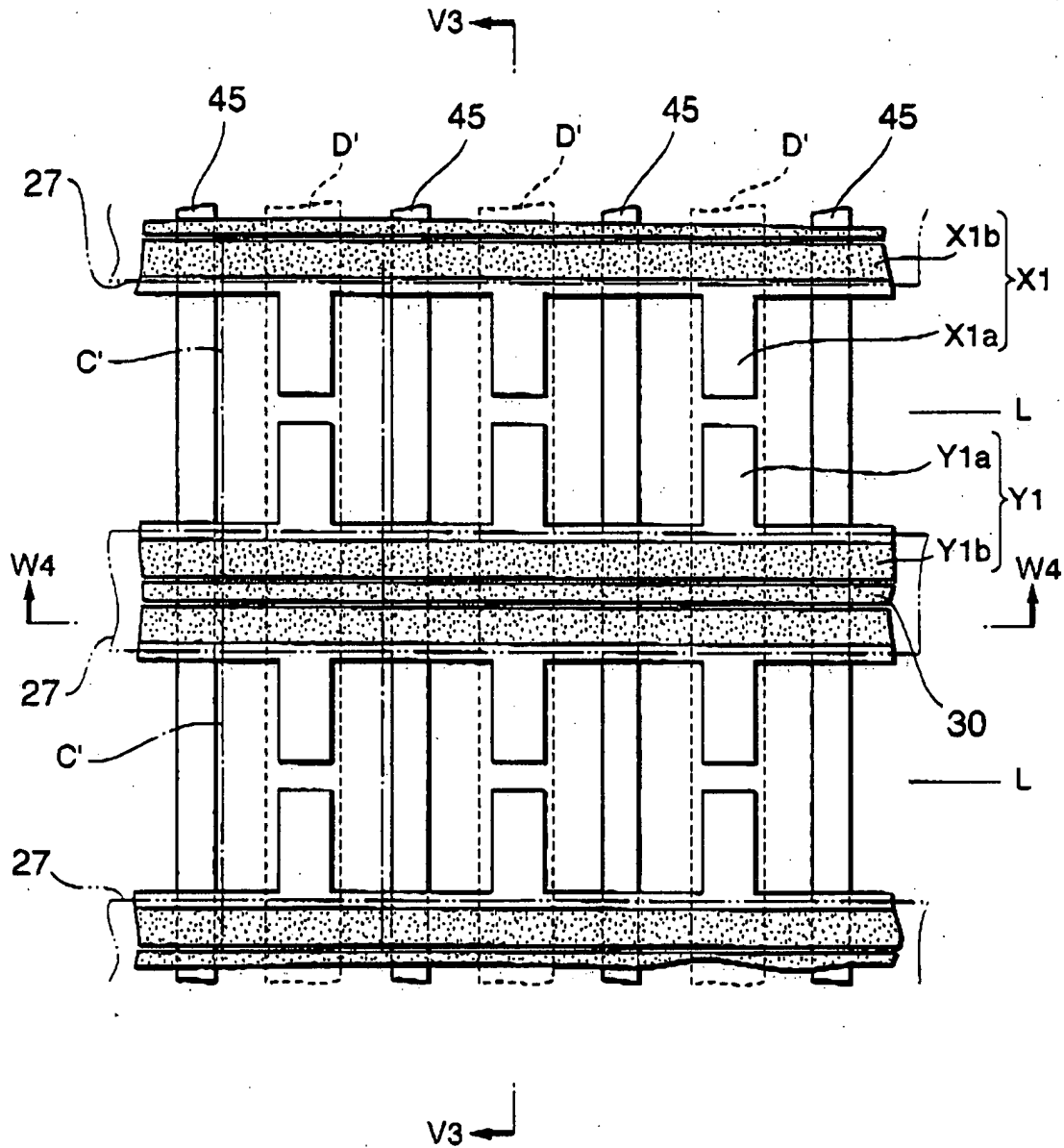


FIG.10

SECTION V3-V3

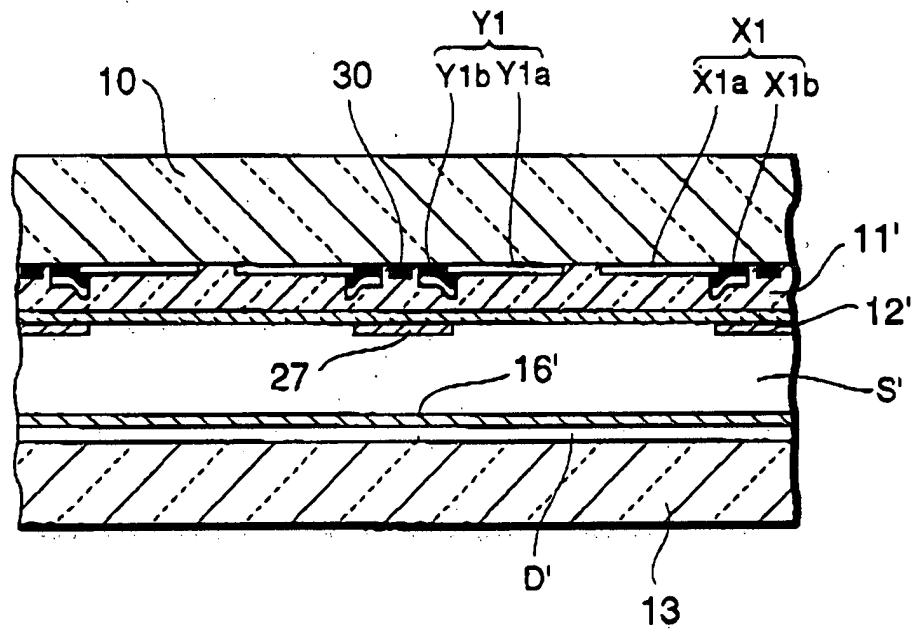


FIG.11

SECTION W4-W4

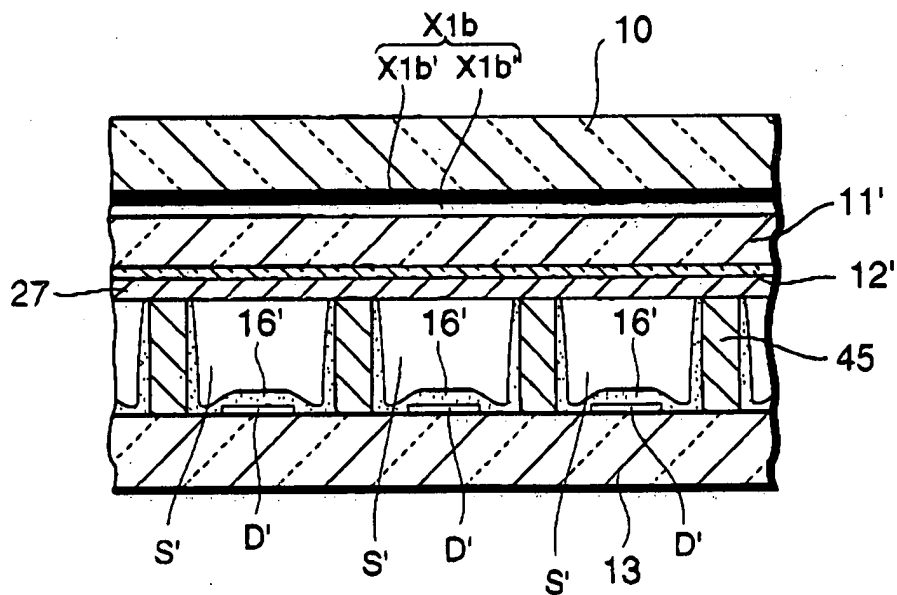
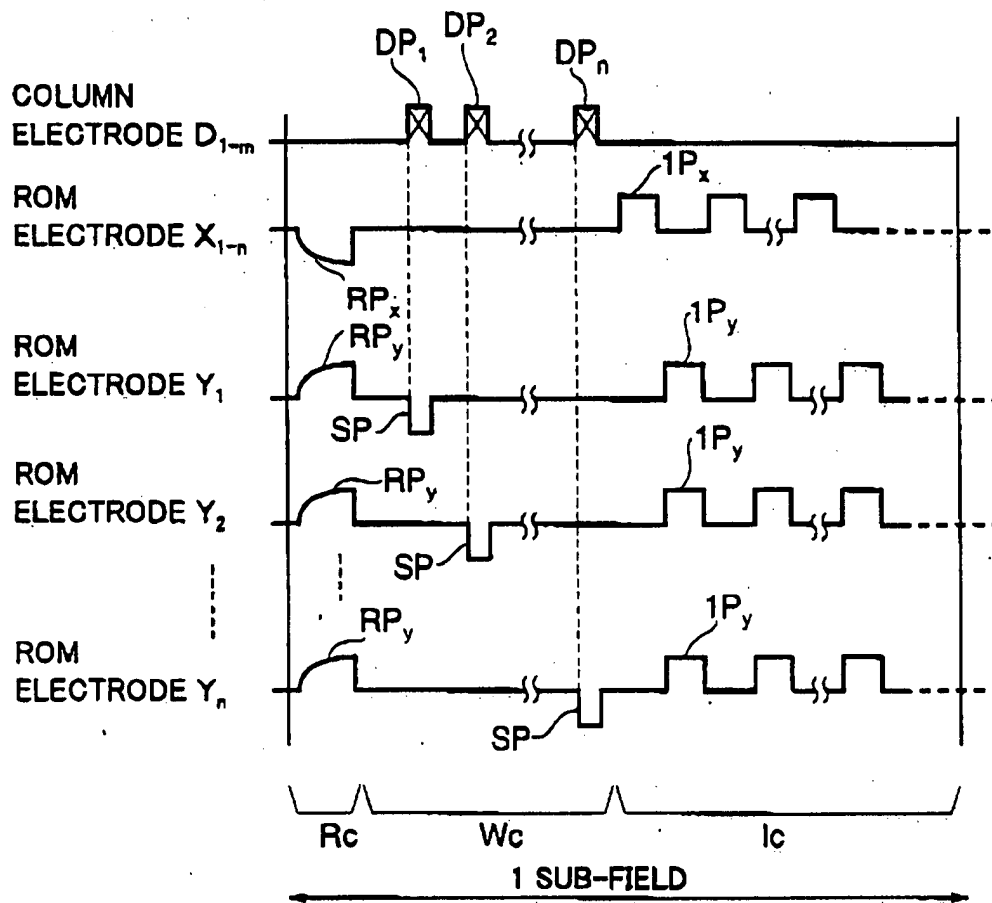


FIG.12



[Name of Document] Abstract

[Summary]

[Object] Provision of a plasma display panel capable of preventing a false discharge to improve the quality of displayed images.

[Means of Solving the Problems] In the plasma display panel having: a front glass substrate 10 on which a plurality of row electrode pairs (X, Y) and a protective layer 12 are provided; and a back glass substrate 13 on which a plurality of column electrodes D are provided so as to form discharge cells C at the intersections of the row electrode pairs and the column electrodes in a discharge space S and which a phosphor layer 16 is provided on the face thereof facing toward the discharge space, a secondary electron emissive layer 17, which is formed of materials having a higher coefficient of secondary electron emission than that of dielectrics forming said protective dielectric layer, is placed at a site facing each discharge cell C between the front glass substrate 10 and the back glass substrate 13.

[Selected Drawing] Fig. 2